

## Frequency generator

- up to 16 channels analog output
- 0.1 Hz – 10 kHz waveforms
- Pulse, Saw, Triangle, Noise, Arbitrary and DC waveforms
- 16 bit, up to 1 MSa/s/ch
- 1024 M-point arbitrary waveforms
- Linear & logarithmic sweeps, step sweeps, burst and chirp operation
- 10 V<sub>pp</sub> amplitude range
- Controllable via DCOM-Interface



## Specifications

Frequency generator		Output channel	
<b>Common Characteristics</b>		Number	up to 16 (more on request)
Gain accuracy	< 0.07 %	Update rate	up to 1MSamples/sec
THD	< 0.05 %	<b>Waveforms</b>	
SNR	> 80 dB	Types	Sine, Square, Saw, Triangle, Noise (White, Pink, Filtered), DC, Arbitrary
Channel separation	> 90 dB @ 10 kHz	<b>Modulation</b>	
Frequency range	100 µHz – 100 kHz	Types	Sweep, Step Sweep, Burst, Chirp
Frequency resolution	100 µHz	<b>Sweep</b>	
Frequency stability	< 2,5 ppm	Waveforms	Sine, Square, Saw, Triangle, Arbitrary
Phase shift resolution	100 µ°	Type	Linear or Logarithmic
Phase coherence (betw. the chs.)	< 100 m°	Sweep time	1 ms to 1000 s
Amplitude range	10 V <sub>pp</sub>	Direction	Up or down
Amplitude Resolution	0,5 mV @ 10 V <sub>pp</sub>	Sweep Mode	Single, loop
DC offset	± 10 V	<b>Step sweep</b>	
DC accuracy	± 2 mV	Waveforms	Sine, Square, Saw, Triangle, Arbitrary
Update rate	1000 kHz/sec/ch @ 2 channels 600 kHz/sec/ch @ 4 channels 300 kHz/sec/ch @ 8 channels 150 kHz/sec/ch @ 16 channels	Direction	Up
<b>Main output</b>		<b>Burst</b>	
Impedance	10 Ohm	Waveforms	Noise
Output current	± 10 mA	Mode	Counted, continuous
Output noise	< 40 µVRMS @ 10 kHz	<b>Chirp</b>	
Protection	Short circuit prot., CPU control via watchdog	Waveforms	Sine, Square, Saw, Triangle, Arbitrary
Connectors	BNC female	Mode	Counted, continuous
<b>Optional FGEN-watchdog</b>		<b>Arbitrary</b>	
Smooth output fade out	Ramp to 0 within 100 msec	Wave form length	2 to 1024 M points
Watchdog time	20 msec to 2 sec		
Interlock input	TTL / CMOS or Isolated		
Interlock output	TTL / CMOS or Isolated		
Programming interface	RS-232 / RS-485		

## Description

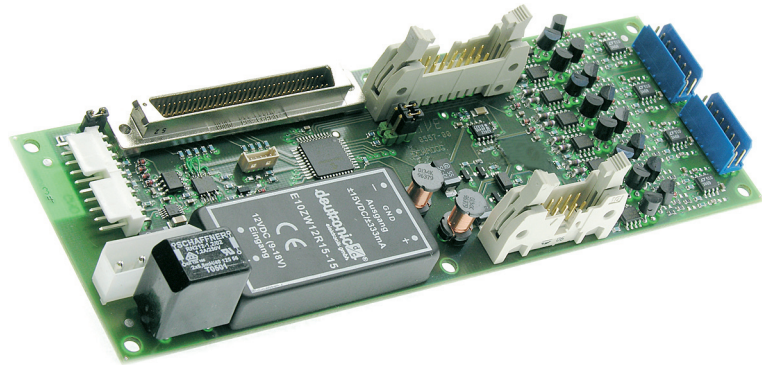
Please refer to DEWESoft online help to get information about the operation.

Visit: <http://www.dewetron.com/at/products/software/dewesoft/and-more/help-tutorials/>

# Internal wiring

## FGEN watchdog (optional)

- Independent from operating system
- Up to 8 channel control
- Input for external control system
- Output for external display, ...
- Signal output divider
- Smooth output fade out

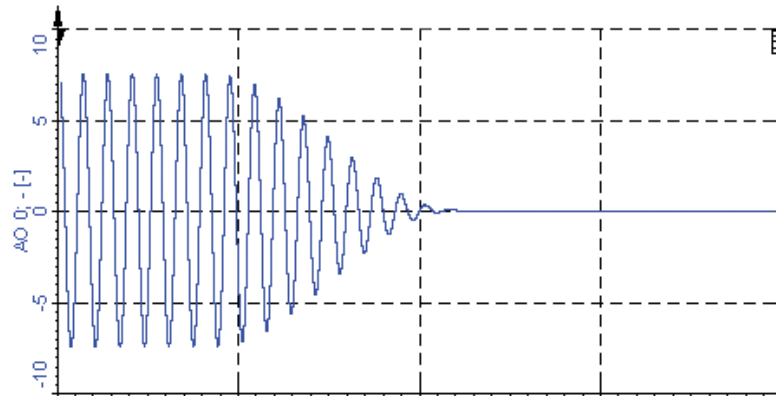


## System specifications

FGEN watchdog	
Analog	
Gain	0 dB, -20 dB
Input voltage range	$\pm 10$ V
Channel separation @ 10 kHz	> 90 dB
Input configuration	Single ended
Input impedance	10 kOhm
Input connector	68-pin Amplimite series (AMP Nr. 174339-6)
Gain accuracy	0.025 % @ 10 V range (0.07% @ 1 V range)
Offset accuracy	1 mV @ 10 V range (0.5mV @ 1 V range)
Output noise @ 10 kHz	< 40 $\mu$ V <sub>RMS</sub>
Output impedance	10 Ohm
Output current	$\pm 10$ mA
Output connector	BNC female
Bandwidth	300 kHz (10 kHz at MDAQ amplifier)
Interlock connector	
Connector	DSUB 9 pin
Non Isolated input	TTL / CMOS compatible
Isolated input	optocoupler input 3 V to 30 V
Non Isolated output	TTL / CMOS compatible
Isolated output	optocoupler output Open collector (max. 50 V / 50 mA)
Common specifications	
Watchdog time	20 msec to 2 sec
Programming interface	RS-232 / RS-485
Power supply	+12 VDC
Power consumption	typ. 8 W

## Description

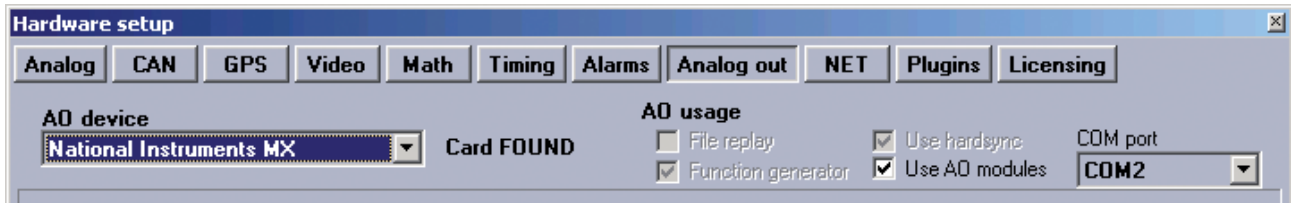
One application for the FGEN is steering a shaker for modal analysis. For protecting the structure mounted on the shaker the FGEN watchdog can be used. The protection is done by permanently checking the communication with the host system. If the communication between watchdog and the host is lost, the correct signal waveform at the output of the FGEN is not guaranteed anymore. In case of this error condition or by control signal at the interlock connector, the output is switched down to zero smoothly by a hardware circuit like shown on the next page.



The state of the watchdog is indicated by two output signals on the interlock connector. In addition this full scale output signal of the AD-board can be divided by 10 allowing to decrease the full scale resolution from  $\pm 10$  Volt to  $\pm 1$  Volt.

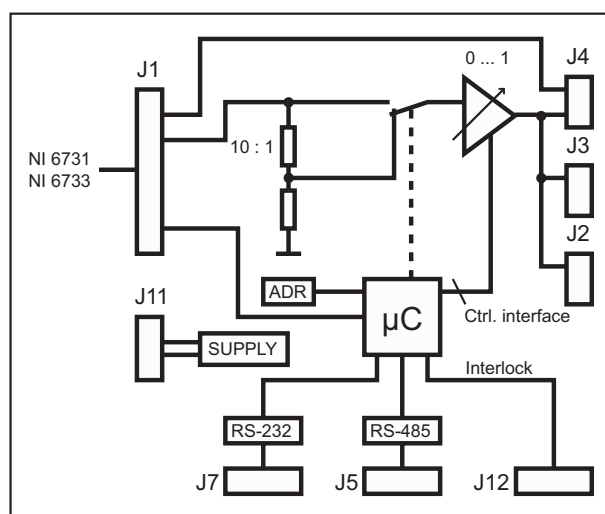
## Software settings

The Watchdog is needs to be enabled inside the hardware setup of DEWESoft like shown below. The COM port number is only a example. Please select the port number.



*Note: Without enabling the Watchdog inside DEWESoft the output signal will be generated.*

## Block diagram



# Internal wiring

The output of the DA-board is connected to J1. The channels are wired to a signal output divider, which is controlled by the onboard microcontroller. The output from the DA-card can either be rooted directly to the security fade out circuit or can be rooted through a signal divider (10:1). This fade out circuit is activated by the  $\mu\text{C}$  if the interlock input becomes active or if the communication of the RS232 (or RS485) is "lost" (not frequently updated) to host system. The output channels are available on J2 and J3 in parallel and are short circuit protected. The reference output signals are wired to J4.

## Pin assignment

**J1**  
68-pin Amplimite series (AMP Nr. 174339-6)

<b>J2/J3</b>	
AOUT0	1 2 GND
AOUT1	3 4 GND
AOUT2	5 6 GND
AOUT3	7 8 GND
AOUT4	9 10 GND
AOUT5	11 12 GND
AOUT6	13 14 GND
AOUT7	15 16 GND

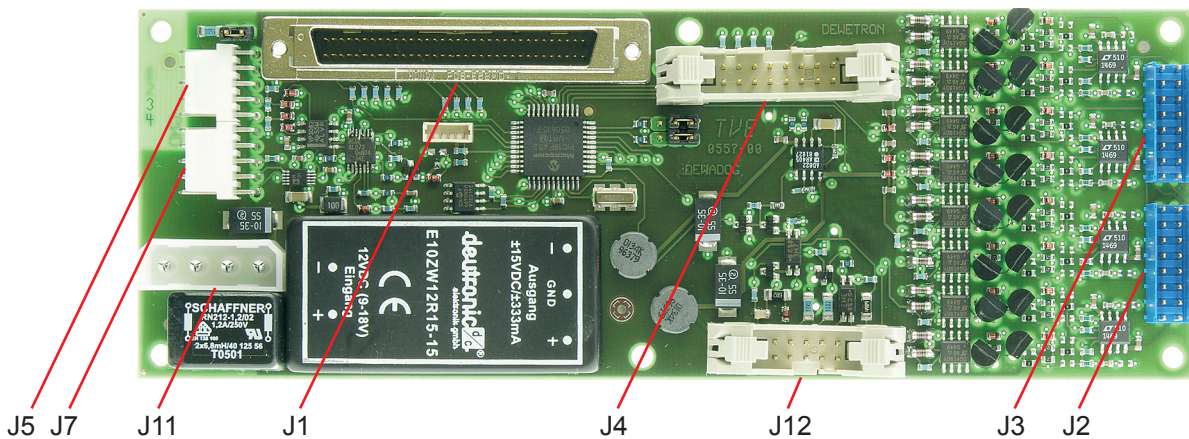
<b>J4</b>	
AOUT4	1 2 GND
AOUT5	3 4 GND
AOUT6	5 6 GND
AOUT7	7 8 GND
DIO4	9 10 DGND
DIO5	11 12 DGND
DIO6	13 14 DGND
DIO7	15 16 DGND

<b>J5</b>	
INT_LOCK	1
RS-485 A	2
N.C.	3
RS-485 B	4
GND	5

<b>J7</b>	
RXD	1
TXD	2
GND	3
N.C.	4
N.C.	5

<b>J12</b>	
Isolated input+	1 2 Isolated input-
TTL/CMOS input+	3 4 TTL/CMOS input-
+5 V <sub>Dc</sub>	5 6 GND
Isolated output+	7 8 Isolated output-
TTL/CMOS output+	9 10 N.C.

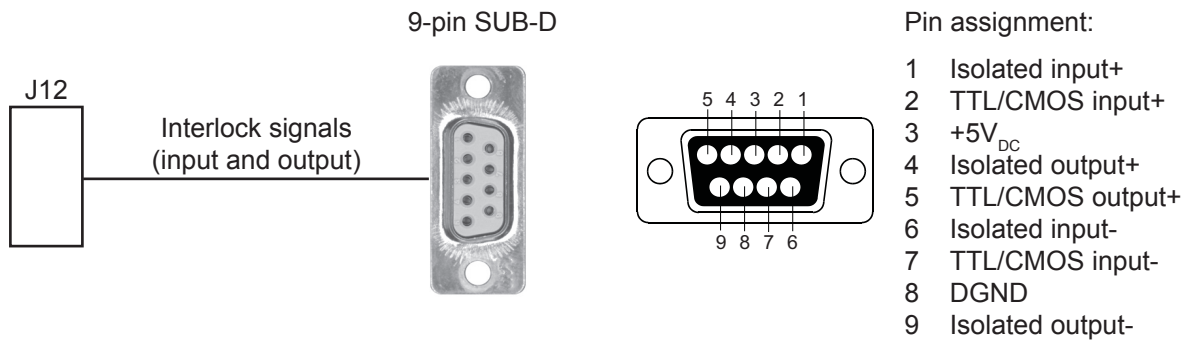
<b>J11</b>	
12 V	1
GND	2
GND	3
N.C.	4



## Interlock connector

The interlock connector contains the interlock signals (input and output) for enabling the out. It is prepared to connect for example the shaker interlock input.

### Block diagram



The isolated input as well as the TTL/CMOS input must have high level for the operation. Otherwise the output is switched off by the fade out circuit. If the interlock circuit is not needed, pin 1,2,3 must be tied together and also pin 6, 7, 8. This simulates a correct "interlock enable".

A correct operation is indicated by a high level on the TTL/CMOS output+. Also the optocoupler output is turned on (isolated output).

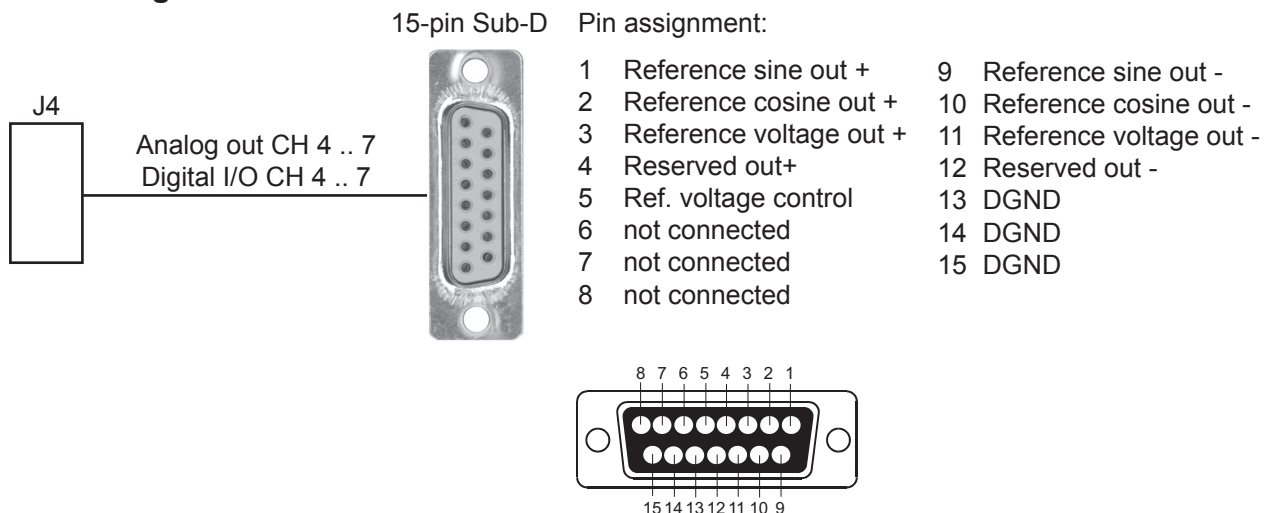
## Reference output (optional)

As an option the data acquisition systems are suited with a reference input connector allowing to "disconnect" automatically all sensors (digitally controlled) and connect an output signal from the FGEN for checking the complete data acquisition system.

The reference output connector on FGEN contains the source signals for this automatic system check. The last four analog output channels of the FGEN (named with sine, cosine, reference and reserved) are wired in parallel to the BNC. The reference voltage control signal (signal DIO4 from DA-Board) is used to switch the DAQ-System to the standard operation mode (high level).

In the calibration mode the reference voltage out is automatically used for the input signal.

### Block diagram



# Internal wiring

---

Notes